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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,686	04/07/2004	Tony J. Tewell	ECCO112.CIP	8528

7590 07/25/2005

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EXAMINER	
GOINS, DAVETTA WOODS	
ART UNIT	**PAPER NUMBER**
2632	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,686	TEWELL ET AL.	
	Examiner	Art Unit	
	Davetta W. Goins	2632	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,9-14 and 16-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,9-14 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 9, 10, 12-14 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morrissey, Jr. et al. (US Pat. 6,452,340 B1) in view of Bell (US Pat. 4,190,830).

In reference to claim 1, Morrissey discloses a) the indicator circuit for a visual warning device, which is met by LED D2 of alarm circuit 64 will be activated after the determination has been made that the lamp 54 is faulty (col. 6, lines 1-35), and b) the claimed visual warning flashing when a voltage from a charging power supply is triggered by a trigger circuit, the trigger circuit conductively connected and responsive to a control circuit; an output device conductively connected and responsive to an indicator element and the trigger circuit, which is met by a starting aid circuit 50 connected to the power supply 56, charged by capacitor C2, used to limit the current to microprocessor circuit 58, alarm LED 64, and trigger circuit 60 (col. 5, lines 9-32). Although Morrissey does not specifically disclose the claimed flashing indicator, he does disclose a transistor Q1 driven on and off by microprocessor 66 such that pulses are used from the transistor to operate lamp 54 for a period of time (col. 5, lines 61-67; col. 6, lines 1-35). Bell discloses a lamp outage indicator circuit; a transistor may be utilized in conjunction with another

voltage sensitive semiconductor device to energize a two terminal indicator device to provide the necessary lamp outage indication (col. 5, lines 17-29). Since both Morrissey and Bell disclose lamp outage detecting devices that provide an indicator of a faulty light, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of using a flashing indicator, as disclosed by Bell, with the system of Morrissey, to ensure that the attention of the user is gained once the fault of the monitored lamp has been detected.

In reference to claim 2, Morrissey discloses the claimed status output device further comprises an LED, which is met by LED D2 of the alarm circuit 64 (col. 6, lines 1-35).

In reference to claim 3, Morrissey discloses the claimed status and function indicator circuit further comprising a transistor, which is met by transistor Q1 driven on and off by microprocessor 66 such that pulses are used from the transistor to operate lamp 54 for a period of time (col. 5, lines 61-67; col. 6, lines 1-35).

In reference to claims 9, 14, 15, 19, Morrissey discloses a) the claimed power source, which is met by power supply 24 (col. 5, lines 1-8), b) the claimed charging power supply, which is met by capacitor C2 (col. 5, lines 9-32), c) the claimed control circuit, which is met by the luminaire starting circuit 22 (Figure 2), and d) the claimed status and function indicator, which is met by LED D2 of alarm circuit 64 will be activated after the determination has been made that the lamp 54 is faulty (col. 6, lines 1-35). Although Morrissey does not disclose the claimed strobe flash

tube conductively connected to the power source and the trigger circuit, he does disclose a transistor Q1 driven on and off by microprocessor 66 such that pulses are used from the transistor to operate lamp 54 for a period of time (col. 5, lines 61-67; col. 6, lines 1-35). Bell discloses a lamp outage indicator circuit; a transistor may be utilized in conjunction with another voltage sensitive semiconductor device to energize a two terminal indicator device to provide the necessary lamp outage indication (col. 5, lines 17-29). Since both Morrissey and Bell disclose lamp outage detecting devices that provide an indicator of a faulty light, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of using a strobe flash tube, such as the transistor disclosed by Bell, with the system of Morrissey, to ensure that the attention of the user is gained once the fault of the monitored lamp has been detected.

In reference to claims 10, Morrissey discloses the claimed voltage regulator conductively connected to the power source, which is met by Zener diode Z1 regulates the voltage to microprocessor circuit 58 and trigger circuit 60 (col. 5, lines 9-32).

In reference to claim 12, Morrissey discloses the claimed trigger circuit, which is met by trigger circuit 60 (col. 5, lines 9-32).

In reference to claim 13, Morrissey discloses the claimed control circuit further comprising a processor, which is met by microprocessor 26 (col. 5, lines 1-8).

In reference to claim 18, Morrissey discloses the claimed status output device further comprises an LED, which is met by LED D2 of the alarm circuit 64 (col. 6, lines 1-35).

3. Claims 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morrissey, Jr. et al. in view of Bell as applied to claim 9 above, and further in view of Tanaka.

In reference to claims 11, 16, neither Morrissey nor Bell disclose the claimed pulse width modulation circuit. However, Morrissey does disclose a microprocessor 66 that sends out a pulse train to trigger circuit 60; the pulses coupled to lamp 54 by transformer T1; the microprocessor 66 waits a predetermined period of time prior to operating lamp 54 (col. 5, lines 60-67; col. 6, lines 1-35). Tanaka discloses lighting equipment that determines the failure of the light source 1; the device includes a timer 680 and timer 682 to generate pulses having predetermined pulse width for generating (col. 4, lines 35-68; col. 4, lines 1-23). Since Morrissey and Tanaka disclose devices that determine the failure of a light and include timers for operating the light, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of using a pulse width modulated signal, as disclosed by Tanaka, with the system of Morrissey, to produce pulse signals that will ensure the operation of the light will occur at controlled and specific times.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-3 and 9-14 and 16-19 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-10 of U.S. Patent No. 6,720,883 B2. Although the conflicting claims are not identical, they are not patentably distinct from each other because it would have been obvious to one of ordinary skill in the art at the time of the invention that claims 9-19 of the present application are clearly disclosed in claims 1-10 of U.S. Patent No. 6,720,883 B2.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Davetta W. Goins whose telephone number is 571-272-2957. The examiner can normally be reached on Mon-Fri with every other Fri. off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Daniel Wu can be reached on 571-272-2964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Davetta W. Goins
Primary Examiner
Art Unit 2632

Davetta W Goins

D.W.G.
July 19, 2005